ROSE CONSULTING ENGINEERS LTD

elsyca electrochemical intelligence

17 Home Farm Avenue
Macclesfield
SK10 3QW
England

Tel: +44 1625 501 054
Mob: +44 7908 257 496
www.rose-consulting.co.uk,
www.elsyca.com
info@rose-consulting.co.uk

CASE STUDY

Title: Bipolar pulsed simulation of a Cu plating process for printed circuit boards

Bath type: Sulphuric acid Cu

Software product: Elsyca PlatingMaster

Industry: Electronics – Printed Circuit Boards

Validity and reliability: Correlation between simulated and measured layer thickness values is well above 90%

Goal of simulations: Determine optimal set of electrical process parameters through simulations

Customer Benefits: Productivity improvements, time & cost savings, more uniform & higher quality product, accurate quoting of jobs

Description:

The copper plating process is one of the most critical steps in the PCB manufacturing process. Although a non-uniform copper deposition inside through-holes, micro-vias and blind holes is determining the yield, also the layer thickness distribution over the entire PCB is highly critical, in particular for multilayer designs. Bipolar pulsed current rectifiers are widely used in the high-end PCB market to reduce fall-out by more uniform deposits in blind and through-holes and on the external layers of the PCB layout.

A distinction can be made between plating tank scale simulations (= macro-scale, figure 1), PCB/pattern scale simulations (= meso-scale, figure 2) and feature scale simulations (= micro-scale). Macro-scale simulations predict the difference in layer thickness from one board to another or from one printed circuit to another printed circuit on the same board. An example of the macro-scale current density distribution is given in figure 3, for normal operating conditions (left) and for another situation with 2 empty anode baskets (right). Remark that the influence of the circuit layout has not been taken into account. Meso-scale simulations however should incorporate the printed circuit layout, since the layout is determining the current and layer thickness distribution on the board. An example of a computed layer thickness distribution of the PCB pattern layout as shown in figure 2 is given in figure 4.

Defining the PCB rack configuration as depicted in figure 1 in Elsyca PlatingMaster is really easy and fast (less than 30 minutes) as is computing the resulting current density distribution (figure 3). A meso-scale simulation of the pattern layout (figure 2) for a bipolar pulsed current signal (with well defined duty cycle, anodic and cathodic pulse amplitude) takes only a few minutes.

Elsyca PlatingMaster can be used to optimize plating configuration issues:

- PCB rack design (macro-scale)
- Number of anodes and positioning (macro-scale)
- Current thieves or background grids (meso-scale)

In most production environments, the plating configuration is rather fixed, hence adding current thieves and background grids to the circuit layout might not always be practical.

However, the electrical process parameters can be adjusted for each PCB series: for DC processes, the total current can be modified; and for bipolar pulsed current signals, the duty cycle, anodic and cathodic current pulse amplitude can be easily determined using the Elsyca software solutions.

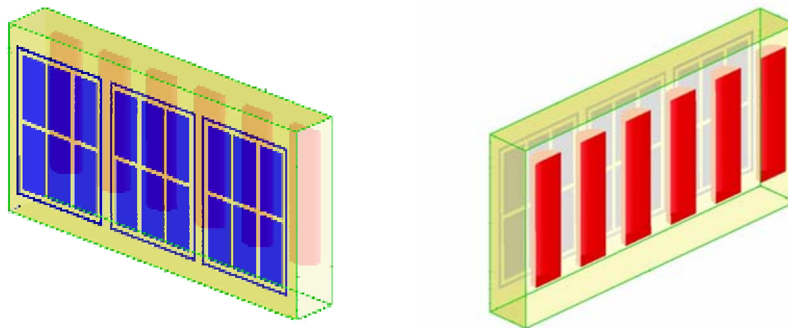

Figure 1: Vertical plating tank configuration with anode baskets (red) and PCB's (blue)

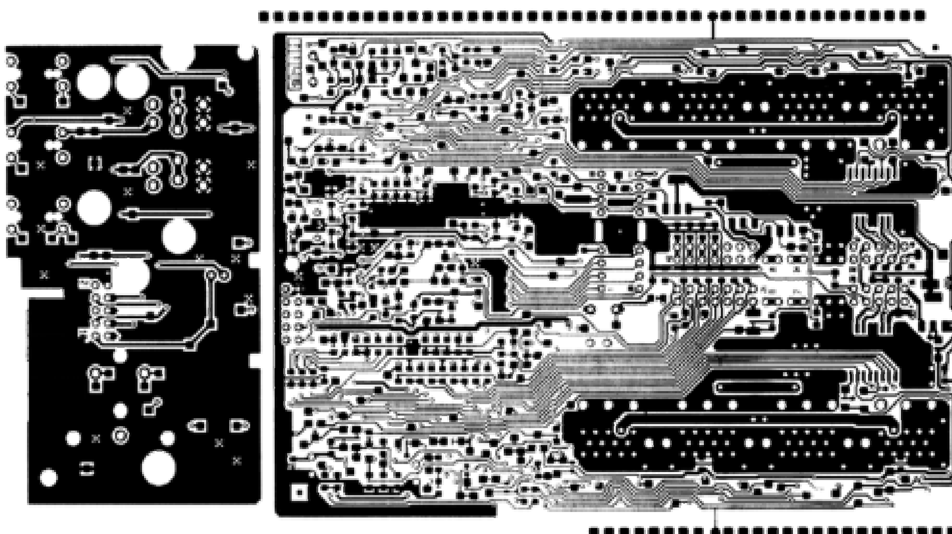

Figure 2: Typical PCB layout

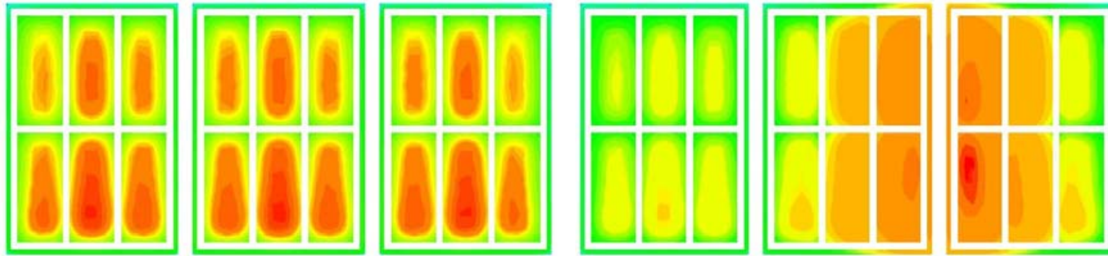

Figure 3: Current density distribution over the PCB surfaces (red corresponds to lowest current densities. Normal operating conditions (left) and situation with two anode baskets empty (right)

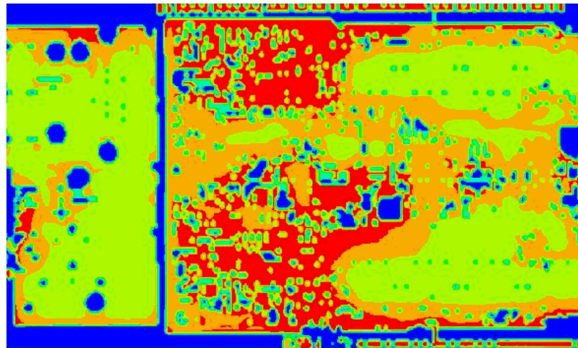

Figure 4: Layer thickness distribution (red corresponds to elevated values) over the PCB